What Is Claimed Is:

1. A method for designing an integrated circuit using a mask-programmable fabric, which contains both mask-programmable logic and a mask-programmable interconnect, the method comprising:

receiving a description of a mask-programmable cell, wherein instances of the mask-programmable cell are repeated to form the mask-programmable fabric;

using the description of the mask-programmable cell to generate a derived library containing cells that can be obtained by programming the mask-programmable cell;

receiving a high-level design for the integrated circuit;

performing a synthesis operation on the high-level design to generate a preliminary netlist for the high-level design that contains references to cells in the derived library; and

converting the preliminary netlist into a netlist that contains references to the mask-programmable cell.

2. The method of claim 1, further comprising performing a placement operation and a routing operation on the netlist to produce a layout for the integrated circuit.

3. The method of claim 2, wherein performing the routing operation involves programming the mask-programmable logic and mask-programmable interconnect.

4. The method of claim 1, wherein the mask-programmable logic and the mask-programmable interconnect that make up the mask-programmable fabric can be programmed by changing inter-metal via layers and/or metal layers

5. The method of claim 1, wherein the method further comprises performing a packing operation on the netlist to combine cells that can use free resources from other cells.

6. The method of claim 5, wherein performing the packing operation involves considering:

drive strengths of output pins for mask-programmable cells;

routability of pins for mask-programmable cells;

net count for mask-programmable cells; and

active pin count for mask-programmable cells.

7. The method of claim 1, wherein the mask-programmable cell includes a sequential logic portion, and wherein the derived library contains a sequential cell, which corresponds the sequential logic portion of the mask-programmable cell.

8. The method of claim 1,

wherein the description of the mask-programmable cell defines one or more pins;

wherein a pin may be specified as being tied to, power, ground, a route segment or another pin;

wherein a pin may be associated with a logic function; and

wherein a pin may be specified as part of a sequential element.

9. The method of claim 8,

wherein the description of the mask-programmable cell defines route segments for routing signals within the mask-programmable fabric;

wherein route segments may be horizontal, vertical or at any angle;

wherein several route segments may be collinear; and

wherein route segments may be coupled to pins or to other route segments.

10. The method of claim 9,

wherein the description of the mask-programmable fabric includes information related to timing for route segments and connections; and

wherein the information related to timing can be used while performing a routing operation for the mask-programmable fabric.

11. A computer-readable storage medium storing instructions that when executed by a computer cause the computer to perform a method for designing an integrated circuit using a mask-programmable fabric, which contains both mask-programmable logic and a mask-programmable interconnect, the method comprising:

receiving a description of a mask-programmable cell, wherein instances of the mask-programmable cell are repeated to form the mask-programmable fabric;

using the description of the mask-programmable cell to generate a derived library containing cells that can be obtained by programming the mask-programmable cell;

receiving a high-level design for the integrated circuit;

performing a synthesis operation on the high-level design to generate a preliminary netlist for the high-level design that contains references to cells in the derived library; and

converting the preliminary netlist into a netlist that contains references to the mask-programmable cell.

12. The computer-readable storage medium of claim 11, wherein the method further comprises performing a placement operation and a routing operation on the netlist to produce a layout for the integrated circuit.

13. The computer-readable storage medium of claim 12, wherein performing the routing operation involves programming the mask-programmable logic and mask programmable interconnect.

14. The computer-readable storage medium of claim 11, wherein the mask-programmable logic and the mask-programmable interconnect that make up the mask-programmable fabric can be programmed by changing inter-metal via layers and/or metal layers.

15. The computer-readable storage medium of claim 11, wherein the method further comprises performing a packing operation on the netlist to combine cells that can use free resources from other cells.

16. The computer-readable storage medium of claim 15, wherein performing the packing operation involves considering:

drive strengths of output pins for mask-programmable cells;

routability of pins for mask-programmable cells;

net count for mask-programmable cells; and

active pin count for mask-programmable cells.

17. The computer-readable storage medium of claim 11, wherein the mask-programmable cell includes a sequential logic portion, and wherein the derived library contains a sequential cell, which corresponds the sequential logic portion of the mask-programmable cell.

18. The computer-readable storage medium of claim 11,

wherein the description of the mask-programmable cell defines one or more pins;

wherein a pin may be specified as being tied to, power, ground, a route segment or another pin;

wherein a pin may be associated with a logic function; and

wherein a pin may be specified as part of a sequential element.

19. The computer-readable storage medium of claim 18,

wherein the description of the mask-programmable cell defines route segments for routing signals within the mask-programmable fabric;

wherein route segments may be horizontal, vertical or at any angle;

wherein several route segments may be collinear; and

wherein route segments may be coupled to pins or to other route segments.

20. The computer-readable storage medium of claim 19,

wherein the description of the mask-programmable fabric includes information related to timing for route segments and connections; and

wherein the information related to timing can be used while performing a routing operation for the mask-programmable fabric.

21. An apparatus that facilitates designing an integrated circuit using a mask-programmable fabric, which contains both mask-programmable logic and a mask-programmable interconnect, the apparatus comprising:

a receiving mechanism configured to receive a description of a mask-programmable cell, wherein instances of the mask-programmable cell are repeated to form the mask-programmable fabric;

a deriving mechanism configured to use the description of the mask-programmable cell to generate a derived library containing cells that can be obtained by programming the mask-programmable cell;

wherein the receiving mechanism is additionally configured to receive a high-level design for the integrated circuit;

a synthesis mechanism configured to perform a synthesis operation on the high-level design to generate a preliminary netlist for the high-level design that contains references to cells in the derived library; and

a conversion mechanism configured to convert the preliminary netlist into a netlist that contains references to the mask-programmable cell.

22. The apparatus of claim 21, further comprising a placement mechanism and a routing mechanism configured to perform a placement operation and a routing operation, respectively, on the netlist to produce a layout for the integrated circuit.

23. The apparatus of claim 22, wherein the routing mechanism is configured to program the mask-programmable logic and mask programmable interconnect.

24. The apparatus of claim 21, wherein the mask-programmable logic and the mask-programmable interconnect that make up the mask-programmable fabric can programmed by changing inter-metal via layers and/or metal layers.

25. The apparatus of claim 21, wherein the apparatus further comprises a packing mechanism configured to perform a packing operation on the netlist to combine cells that can use free resources from other cells.

26. The apparatus of claim 25, wherein performing the packing operation involves considering:

drive strengths of output pins for mask-programmable cells;

routability of pins for mask-programmable cells;

net count for mask-programmable cells; and

active pin count for mask-programmable cells.

27. The apparatus of claim 21, wherein the mask-programmable cell includes a sequential logic portion, and wherein the derived library contains a sequential cell, which corresponds the sequential logic portion of the mask-programmable cell.

28. The apparatus of claim 21,

wherein the description of the mask-programmable cell defines one or more pins;

wherein a pin may be specified as being tied to, power, ground, a route segment or another pin;

wherein a pin may be associated with a logic function; and

wherein a pin may be specified as part of a sequential element.

29. The apparatus of claim 28,

wherein the description of the mask-programmable cell defines route segments for routing signals within the mask-programmable fabric;

wherein route segments may be horizontal, vertical or at any angle;

wherein several route segments may be collinear; and

wherein route segments may be coupled to pins or to other route segments.

30. The apparatus of claim 29,

wherein the description of the mask-programmable fabric includes information related to timing for route segments and connections; and

wherein the information related to timing can be used while performing a routing operation for the mask-programmable fabric.

31. An integrated circuit created through a process that uses a mask-programmable fabric to design the integrated circuit, wherein the mask-programmable fabric contains both mask-programmable logic and a mask-programmable interconnect, the process comprising:

receiving a description of a mask-programmable cell, wherein instances of the mask-programmable cell are repeated to form the mask-programmable fabric;

using the description of the mask-programmable cell to generate a derived library containing cells that can be obtained by programming the mask-programmable cell;

receiving a high-level design for the integrated circuit;

performing a synthesis operation on the high-level design to generate a preliminary netlist for the high-level design that contains references to cells in the derived library; and

converting the preliminary netlist into a netlist that contains references to the mask-programmable cell.

32. A mask for use in an optical lithography process for manufacturing an integrated circuit, wherein the mask is generated through a process that uses a mask-programmable fabric to design the integrated circuit, wherein the mask-programmable fabric contains both mask-programmable logic and a mask-programmable interconnect, the process comprising:

receiving a description of a mask-programmable cell, wherein instances of the mask-programmable cell are repeated to form the mask-programmable fabric;

using the description of the mask-programmable cell to generate a derived library containing cells that can be obtained by programming the mask-programmable cell;

receiving a high-level design for the integrated circuit;

performing a synthesis operation on the high-level design to generate a preliminary netlist for the high-level design that contains references to cells in the derived library; and

converting the preliminary netlist into a netlist that contains references to the mask-programmable cell.